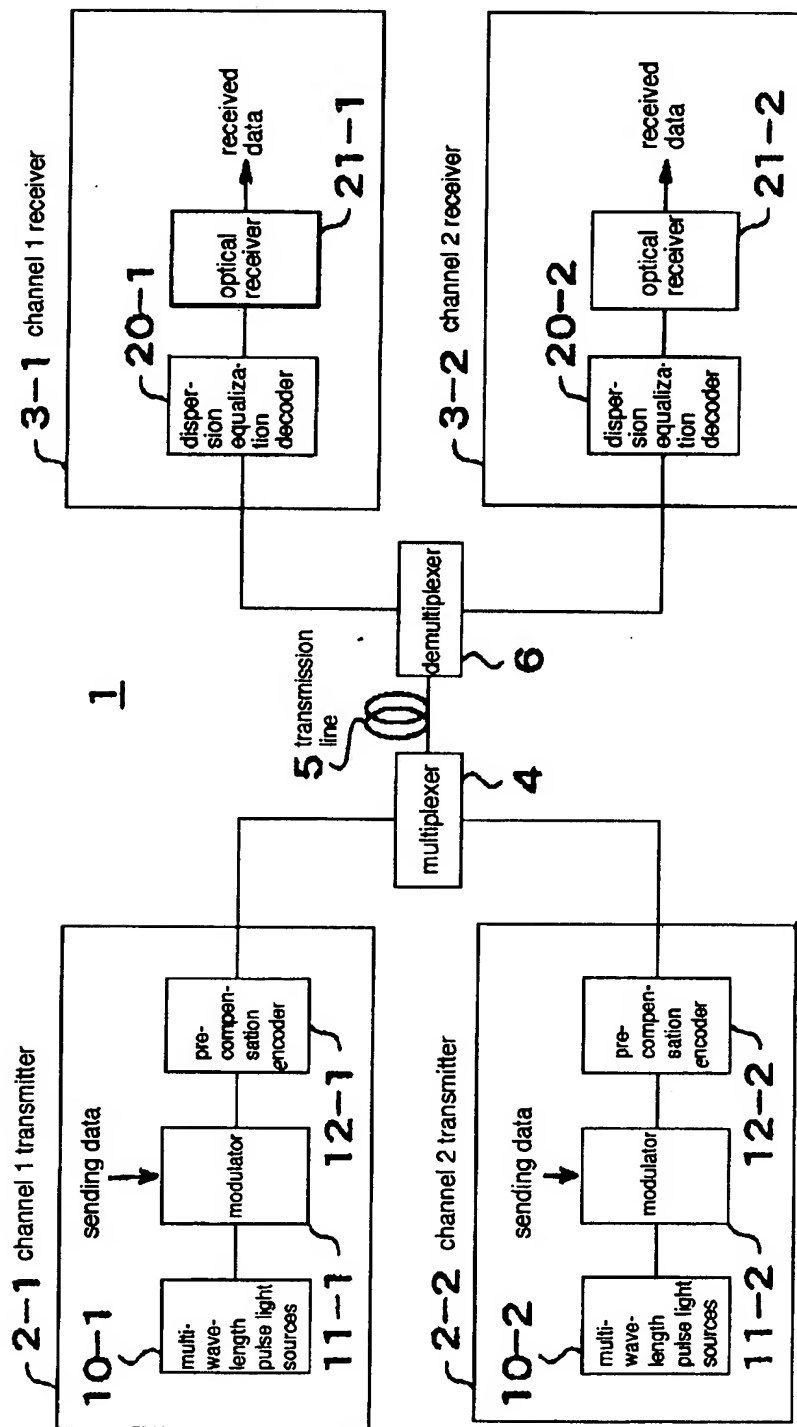


FIG. 1



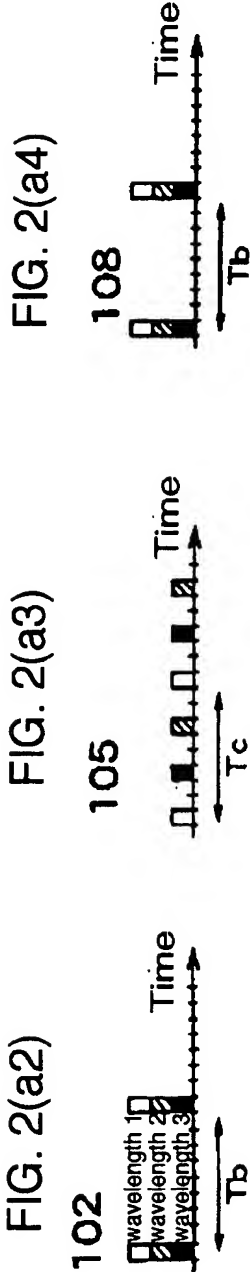
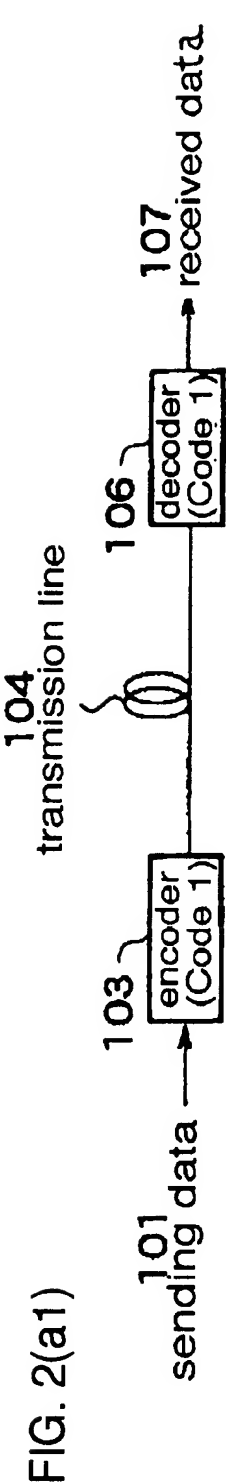


FIG. 2(a3)

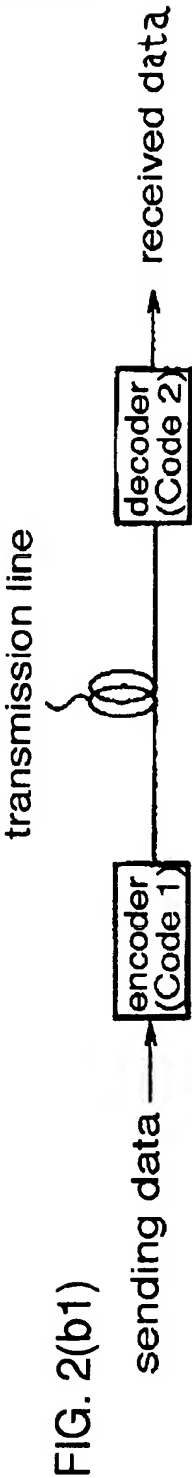


FIG. 2(b2)

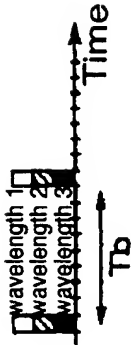


FIG. 2(b3)



FIG. 2(b4)



FIG. 3(a)

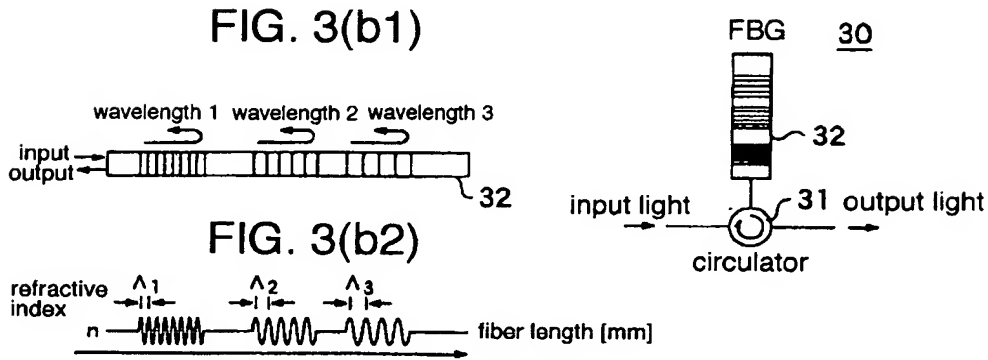


FIG. 4(a)

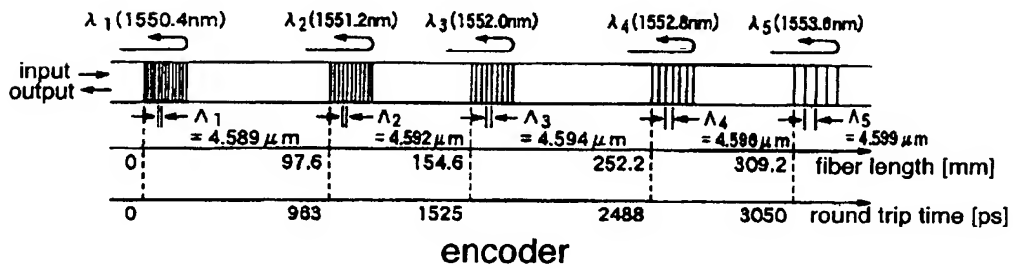


FIG. 4(b)

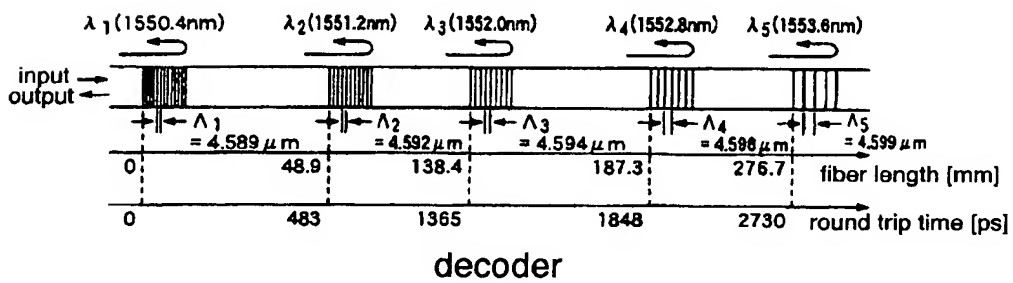


FIG. 5

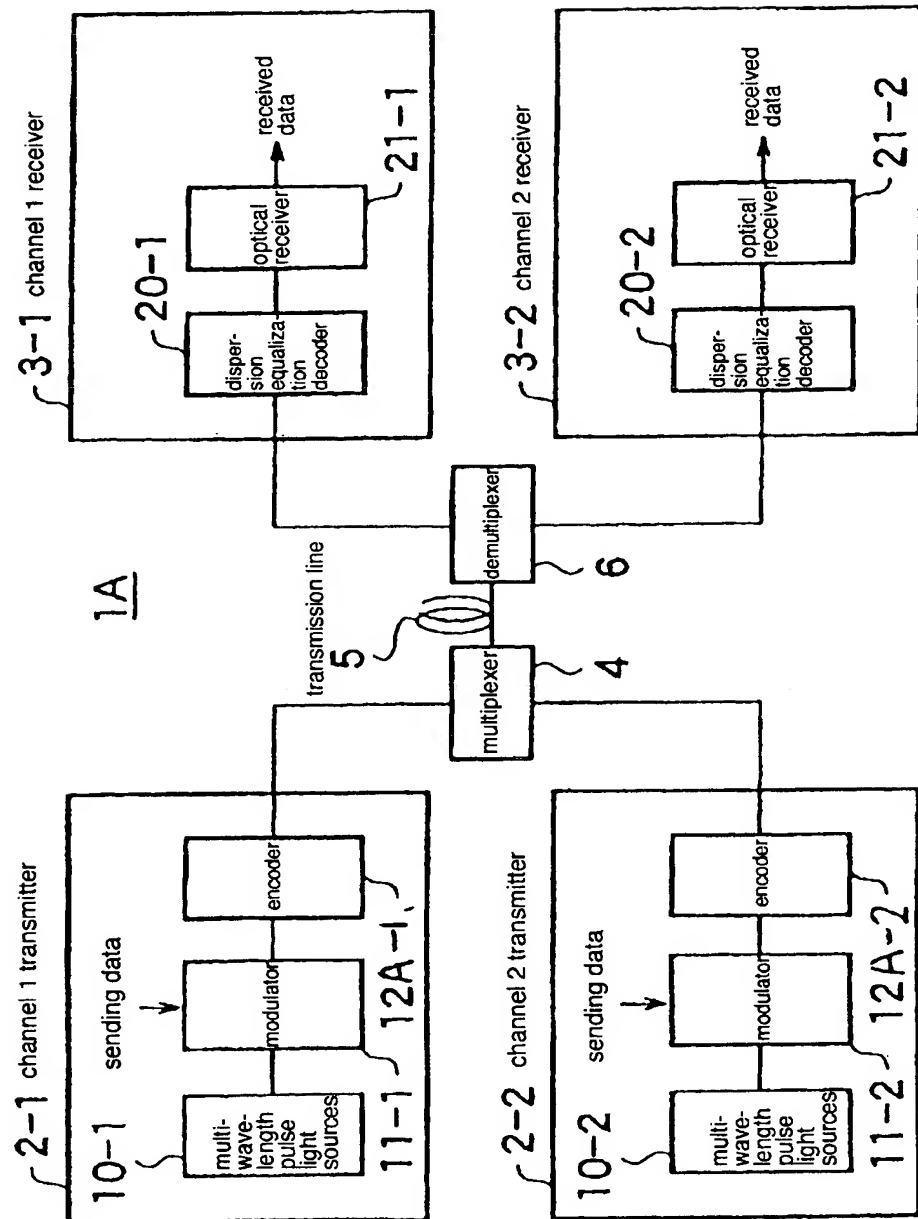


FIG. 6(a)

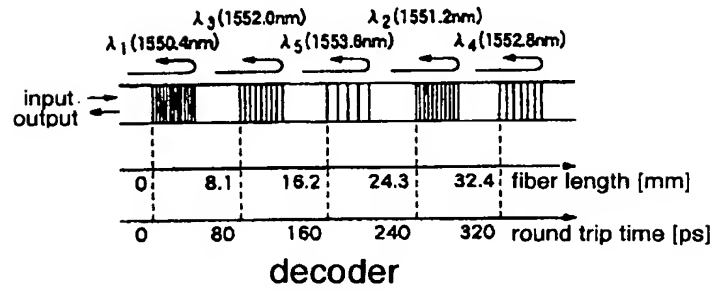


FIG. 6(b)

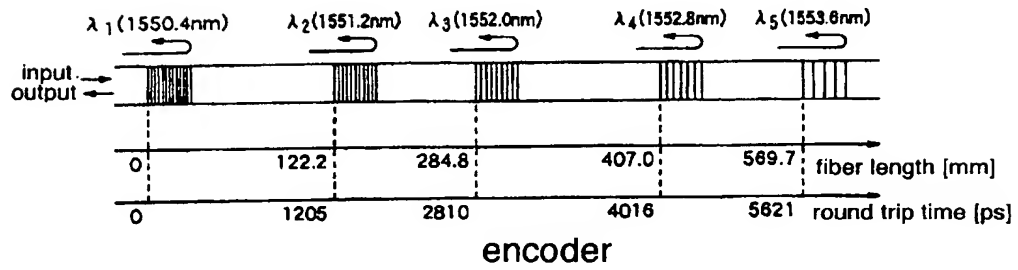


FIG. 7

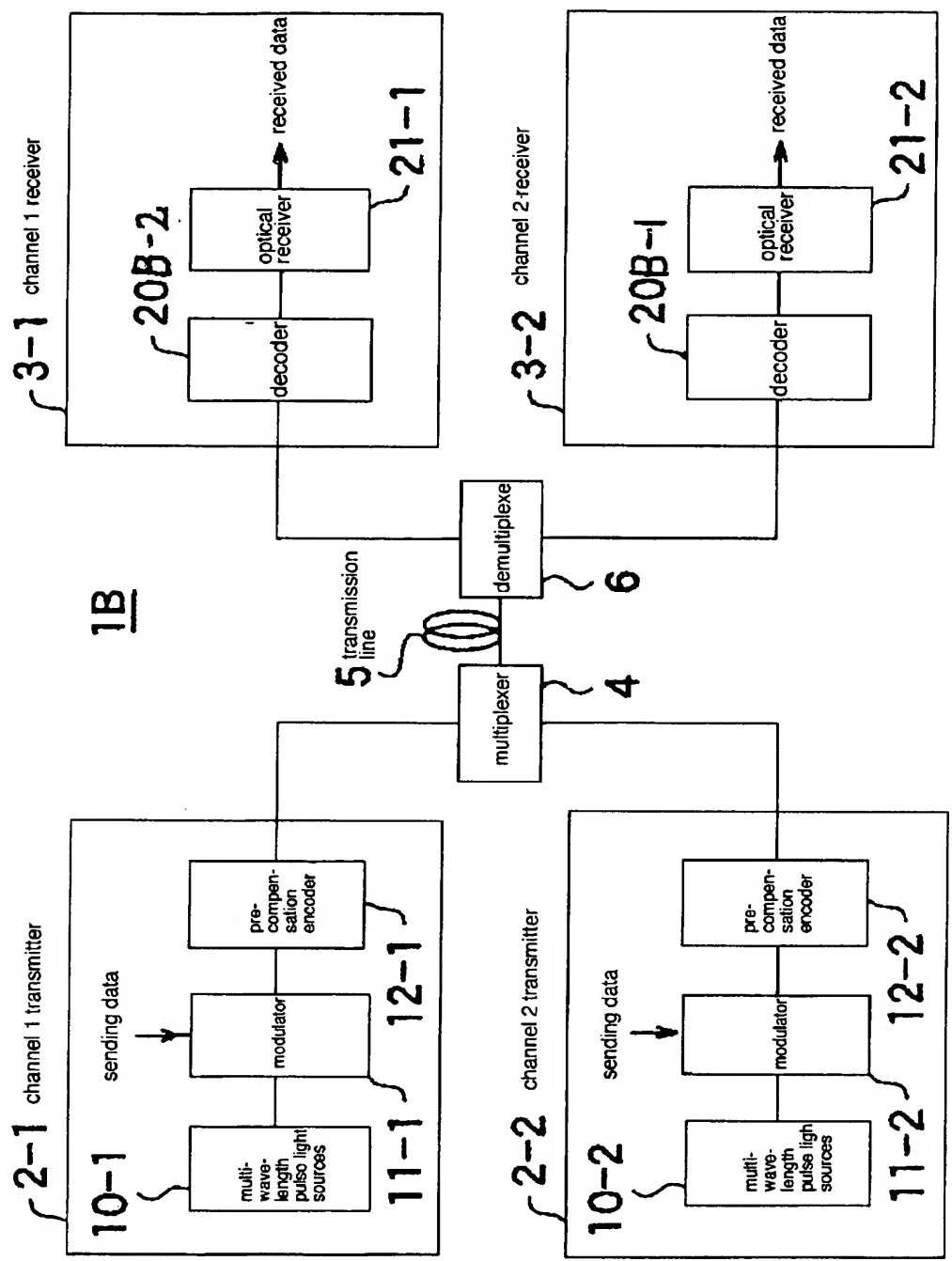


FIG. 8(a)

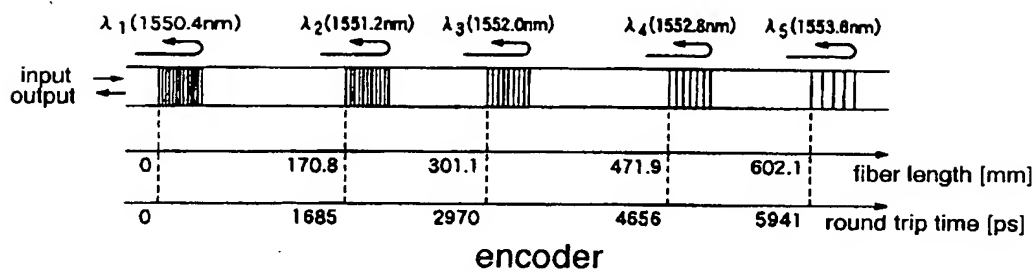


FIG. 8(b)

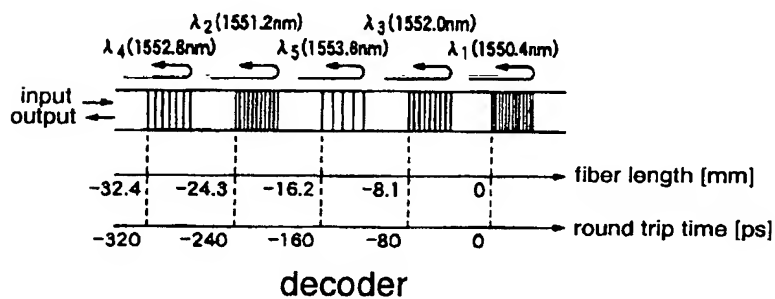
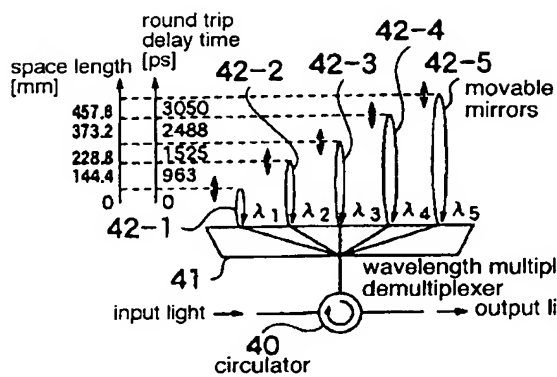
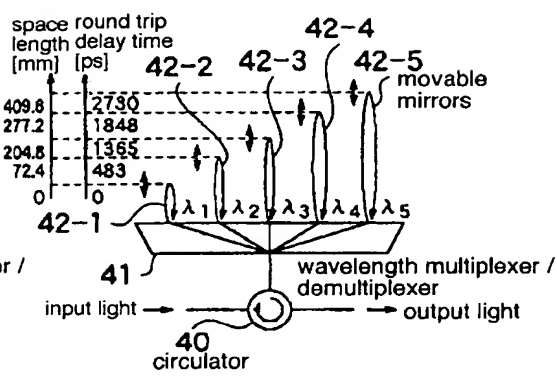


FIG. 9(a)



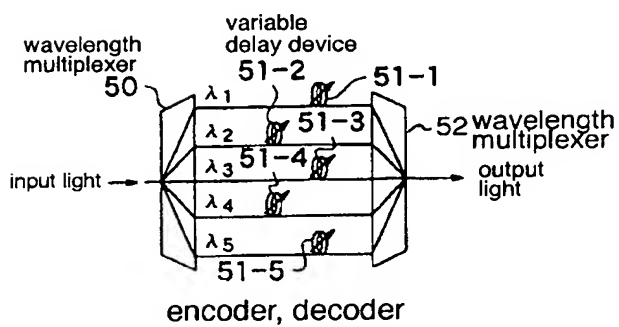
encoder

FIG. 9(b)



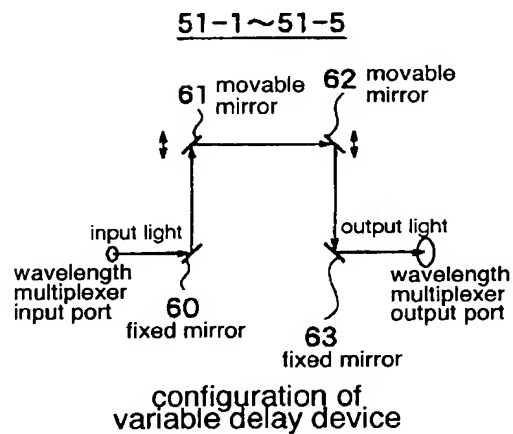
decoder

FIG. 10(a)



encoder, decoder

FIG. 10(b)



configuration of variable delay device